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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,031	CIOACA, DUMITRU	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-43 is/are pending in the application.

4a) Of the above claim(s) 14,18-23,27-35 and 38 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13,15-17,24-26,36,37 and 39-43 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02 May 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. 3/24/05.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 43 are presented for examination.

Election/Restrictions

2. During a telephone conversation with Mr. Thomas J. D'Amico [reg. # 28371] on 24 March 2005 a provisional election was made without traverse to prosecute the invention of Group- I, claims 1-13,15-17,24-26, 36-37,and 39-43. Affirmation of this election must be made by applicant in replying to this Office action. Claims 14, 18-23, 27-35 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-13,15-17,24-26, 36-37,and 39-43, drawn to a power supply control, classified in class 713, subclass 300.

II. Claims 14,19-23, and 27-35, drawn to a charge pump control, classified in class 327, and subclass 148,157,536,538.

III. Claims 18, and 38, drawn to a memory powering, classified in class 365, subclass 226.

4. Inventions I, II, and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as power supply control. In the instant case, invention II has separate utility such as charge pump control. In the instant case, invention III has separate utility such as memory or storage device powering. See MPEP § 806.05(d).

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

6. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II or III, and search required for Group II is not required for Group I or III, and search required for Group III is not required for Group I or II, restriction for examination purposes as indicated is proper.

7. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

8. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the integrated circuit with claimed limitations as claimed in independent claim 43 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

9. The integrated circuit with claimed limitations as claimed in independent claim 43 is not supported in specifications.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1 – 13, 15 – 17, 24 – 26, 36, and 39 – 43 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hosono et al. [hereinafter as Hosono], US Patent 6,404,274 B1.

11. As to claim 1, Hosono teaches a circuit and a method of controlling [setting] a power supply [70, charge pump] comprising:

a. reading a digital signal on a digital data bus [data read is inherent to memory system, col. 13, lines 31 – 32];

b. generating a control signal [generating N1 voltage] in relation to said digital signal [B1,...Bn];

c. feeding [via OPAMP 13] said control signal [N1 voltage] forward to a power supply [70]; and

d. modifying [with first and second voltage setting circuits] a power output [Vxx] of said power supply [70] in response to said control signal [N1 voltage] in anticipation of a changing power demand of a load [load resistor] responsive to [in accordance with] said digital signal [in accordance with digital data][abstract, co. 5, lines 45 – 64, col. 7, lines 1 – 5, col. 8, lines 22 – 67, col. 9, lines 1 – 22, col. 12, lines 19 – 67, col. 13, lines 1 – 11, fig. 2].

12. As to claim 15, Hosono teaches a circuit and a method of controlling [setting] a power supply [70, charge pump] comprising:

a. producing an analog signal [input current/node voltage] related to a number of bits having a particular logic state [H High, L Low] in a digital signal [B1,..

Bn], said analog signal [input current] being independent of an output [Vxx] of said power supply [70];

b. producing an analog signal [input current/node voltage] related to said number of bits [number of bits logic state H, L]; and

c. setting an output [Vxx] of said power supply [70] to a particular level in response to said analog signal [current signal][col. 7, lines 1 – 11, col. 8, lines 22 – 67, col. 9, lines 1 – 22, col. 12, lines 10 – 67, col. 13, lines 1 – 11, fig. 2].

13. As to claim 24, Hosono teaches a circuit and a method of controlling [setting] a power supply [70, charge pump] comprising:

a. sensing a number of bits [by sense operation] in a particular logic state [H high or L low] in a particular digital communication [col. 13, lines 31 – 32]; and

b. adapting [setting] said power supply [70] to supply a particular level [magnitude] of current, said level [magnitude] of current being proportional to said number of bits][col. 7, lines 1 – 11, col. 8, lines 22 – 67, col. 9, lines 1 – 22, col. 12, lines 10 – 67, col. 13, lines 1 – 11, fig. 2].

14. As to claim 39, Hosono teaches a circuit and a method of controlling [setting] a power supply [70, charge pump] comprising:

a. a plurality of data bus inputs [plurality of data bus inputs are inherent to memory];

b. a plurality of outputs [plurality of outputs are inherent to memory]; and

c. a sensing circuit [62 sense amplifier] adapted to activate [control] one or more of said plurality of outputs in response to a corresponding pattern of data bus

signals detected [by decoder 65] on said plurality of data bus inputs [col. 13, lines 27 – 44, fig. 2, 4].

15. As to claim 41, Hosono teaches a circuit and a method of controlling [setting] a power supply [70, charge pump] for data write/erase for a memory [col. 1, lines 6 – 14] comprising:

a. a microprocessor [processor is inherent to write data in memory];

b. a data bus, said data bus connected to said microprocessor [data bus and connection to processor is inherent to data write/erase for a memory]; and

c. an electronic memory device [semiconductor memory, EEPROM] having a plurality of data bus inputs connected to said data bus, said electronic memory device including a power supply controller having a plurality of outputs and a sensing circuit adapted to activate one or more of the plurality of outputs in response to a pattern of data bus signals detected on said plurality of data bus inputs [col. 11, lines 27 – 67, col. 12, lines 1 – 67, col. 13, lines 1 – 36, and 58 – 63, col. 14, lines 1 – 15, and 36 – 67, fig. 2, 6].

16. As to claim 43, Hosono discloses semiconductor integrated circuit comprising:

a. a processing portion [processing portion is inherent to processing (setting of values)][col. 11, lines 24 – 26]; and

b. a memory portion connected to said processing portion by a data bus portion [fig. 4], said memory portion including a power supply and power supply controller [681-683], said power supply controller having a plurality of data bus inputs connected to said data bus portion, an output connected to said power supply, and a

sensing circuit [62] adapted to activate or deactivate said output in response to a corresponding pattern of data [as shown in col. 12, lines 50 – 63] bus signals detected on said plurality of data bus inputs [col. 13, lines 5 – 67, col. 14, lines 1 – 12, lines 24 – 45, fig.4][col. 11, lines 27 – 67, col. 12, lines 1 – 67, col. 13, lines 1 – 36, and 58 – 63, col. 14, lines 1 – 15, and 36 – 67, fig. 2, 6].

17. Claim 37 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Lee, US Patent 6,653,888 B2.

18. As to claim 37, Lee discloses a power supply apparatus [internal voltage generator] comprising:

a. a plurality of charge [voltage] pump circuits [140_m, fig. 2];

b. an input bus having a plurality of input lines [input bus having plurality of input lines is inherent to memory];

c. a control circuit [200, control unit] connected to said input bus, said control circuit adapted to provide a particular plurality of output signals [S1, S2,..] in response to a number of zero bits in an input signal transmitted on said input lines;

d. a plurality of outputs [S1, S2,..] of said control circuit [200], said plurality of outputs being operatively connected to said plurality of charge pump circuits [140_m] respectively, said outputs being adapted to transmit said plurality of output signals to said plurality of charge pumps respectively, whereby said plurality of charge pump are each activated or deactivated in response to said respective plurality of output signals [col. 2, lines 2 – 30, lines 52 – 67, col. 3, lines 18 – 44, col. 4, lines 27 – 67, fig. 2].

19. Claims 39 – 43 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hubber, US Patent 6,421,297 B1.

20. As to claims 39, 41, and 43 Hubber discloses a plurality of data bus inputs [i1, i2, i3], a plurality of outputs [outputs of drivers 326, 328, 330 to data bus 102], and sensing circuit [342, compensation Logic, fig. 5] and, a sensing circuit [342] adapted to activate one or more of said plurality of outputs to a corresponding data pattern of data bus signals detected on said plurality of data bus inputs [abstract, col. 1, lines 8 – 12, col. 3, lines 52 – 67, col. 4, lines 1 – 67, col. 5, lines 1 – 30, col. 7, lines 9 – 60, fig. 3, 5].

21. As to claims 2, and 3, Hosono teaches a plurality of charge pump circuits [681-683, high voltage generating circuits] and clock generating circuits [oscillatior circuits], operatively connected to and adapted to drive respective charge pump circuits [681-683], and enabling of clock circuits and thereby driving respective charge pump circuits [681-683] [col. 5, lines 45 – 64, col. 13, lines 5 – 11, lines 58 – 64, col. 14, lines 4 – 60, fig. 4 – 6].

22. As to claim 4, Hosono teaches the internal voltage generating circuit for nonvolatile semiconductor memory, which inherently teaches parallel data bus configuration too.

23. As to claim 5, Hosono discloses that the control signal is a digital signal [col. 8, lines 36 – 55].

24. As to claims 6, and 7, Hosono discloses a method of controlling power supply [controlling an output Vxx of 70 to a particular level], in response to said analog signal

[current signal][col. 7, lines 1 – 11, col. 8, lines 22 – 67, col. 9, lines 1 – 22, col. 12, lines 10 – 67, col. 13, lines 1 – 11, fig. 2][col. 8, lines 36 – 55].

25. As to claim 8, Hosono teaches the internal voltage generating circuit for nonvolatile semiconductor memory including four bits of data [col. 2, lines 47 – 53].

26. As to claims 9, and 10, Hosono discloses generating voltage signal by flowing an electrical current [I10+I20] through a voltage divider [as shown in fig.2] circuit with plurality of resistors shunted by a plurality of transistors [fig. 2, 6] [col. 7, lines 1 – 11, col. 8, lines 22 – 67, col. 9, lines 1 – 22, col. 12, lines 10 – 67, col. 13, lines 1 – 11, fig. 2][col. 8, lines 36 – 55].

27. As to claims 11, and 12, Hosono discloses a digital memory including Flash memory [col. 1, lines 15 – 20, 39 – 42].

28. As to claim 13, Hosono discloses internal voltage generating required to write [store] or erase data for a Flash memory, which inherently includes to store digital signal as a data word [col. 1, lines 15 – 20, 39 – 42].

29. As to claims 16 and 17, Hosono discloses activating of one or more of a plurality of subcircuits including enabling a clock circuit connected to drive respective charge pumps circuit [col. 5, lines 45 – 64, col. 13, lines 5 – 11, lines 58 – 64, col. 14, lines 4 – 60, fig. 4 – 6].

30. As to claims 25, and 26, Hosono discloses power supply switchingly connecting one or more of plurality of power supply portions includes a charge pump circuit to a load circuit [col. 5, lines 44 – 64, fig. 4].

31. As to claim 40, Hosono discloses power supply controller comprises a charge pump circuit connected to one of plurality of outputs [col. 5, lines 44 – 64, fig. 4].

32. As to claim 42, Hosono discloses an electronic [digital memory including Flash memory] [col. 1, lines 15 – 20, 39 – 42] comprises a charge pump circuit connected to one of plurality of outputs [col. 5, lines 44 – 64, fig. 4].

33. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

34. **Prior Art not relied upon**: Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am - 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
April 4, 2005

JOHN R. COTTINGHAM
PRIMARY EXAMINER